FIG. 1
PRIOR ART

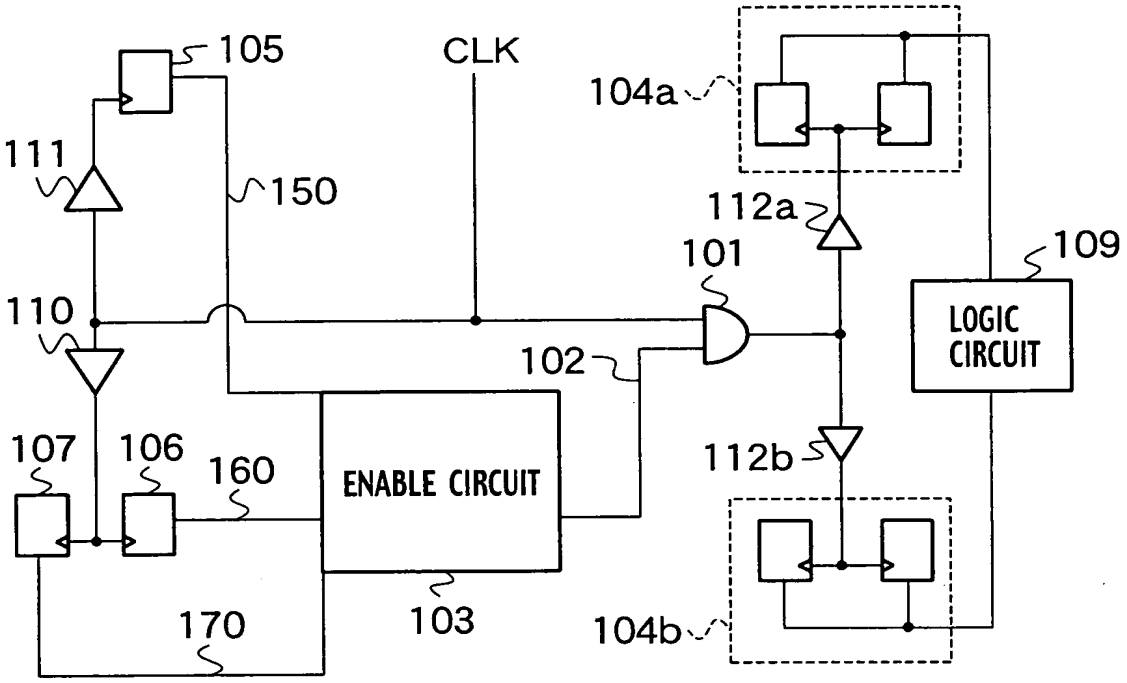


FIG. 2

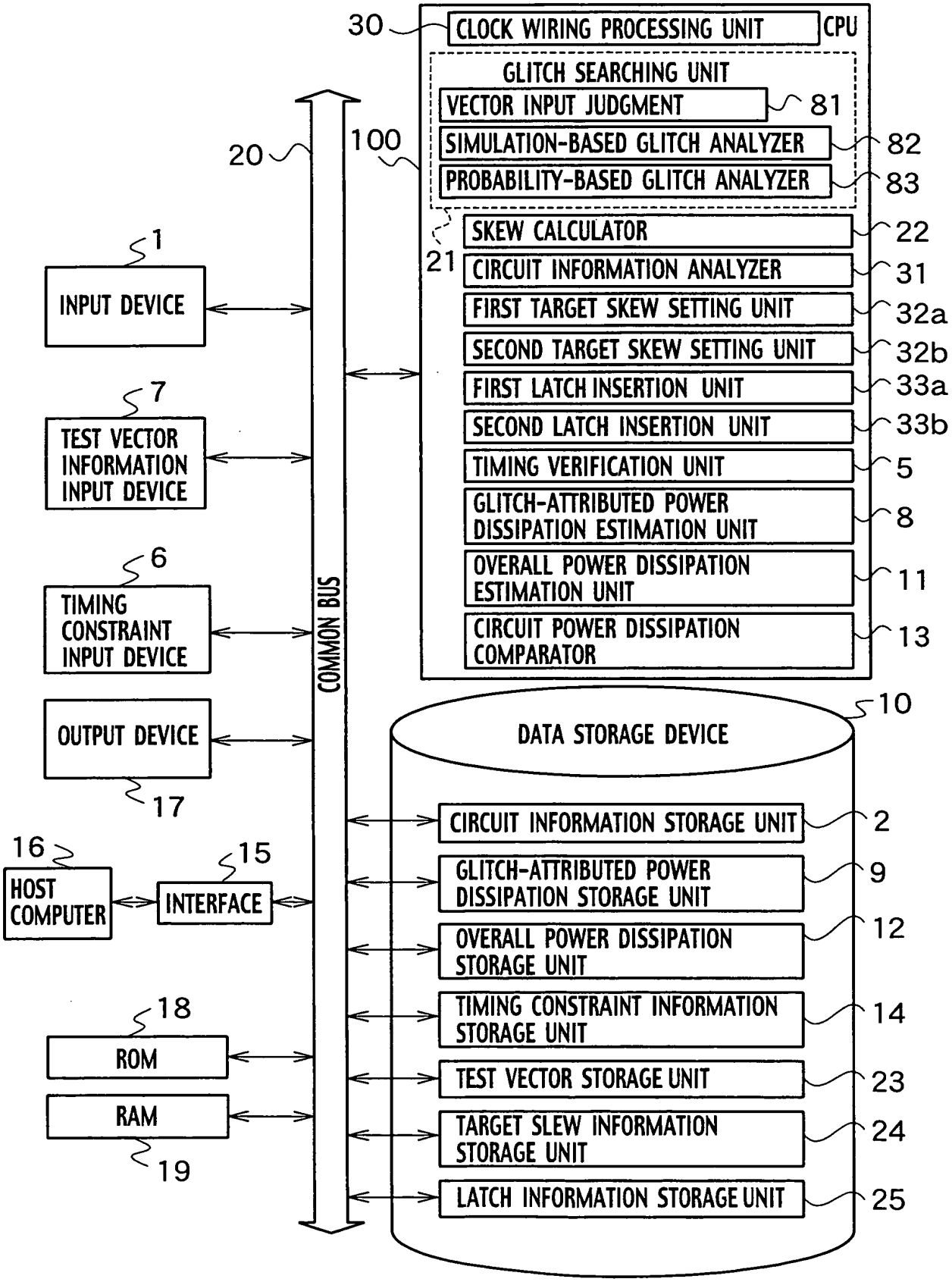

30
CLOCK WIRING PROCESSING UNIT
CPU
GLITCH SEARCHING UNIT
VECTOR INPUT JUDGMENT
81
SIMULATION-BASED GLITCH ANALYZER
82
PROBABILITY-BASED GLITCH ANALYZER
83
100
20
21
SKEW CALCULATOR
22
CIRCUIT INFORMATION ANALYZER
31
FIRST TARGET SKEW SETTING UNIT
32a
SECOND TARGET SKEW SETTING UNIT
32b
FIRST LATCH INSERTION UNIT
33a
SECOND LATCH INSERTION UNIT
33b
TIMING VERIFICATION UNIT
5
GLITCH-ATTRIBUTED POWER DISSIPATION ESTIMATION UNIT
8
OVERALL POWER DISSIPATION ESTIMATION UNIT
11
CIRCUIT POWER DISSIPATION COMPARATOR
13
1
INPUT DEVICE
7
TEST VECTOR INFORMATION INPUT DEVICE
6
TIMING CONSTRAINT INPUT DEVICE
OUTPUT DEVICE
17
COMMON BUS
DATA STORAGE DEVICE
10
CIRCUIT INFORMATION STORAGE UNIT
2
GLITCH-ATTRIBUTED POWER DISSIPATION STORAGE UNIT
9
OVERALL POWER DISSIPATION STORAGE UNIT
12
TIMING CONSTRAINT INFORMATION STORAGE UNIT
14
TEST VECTOR STORAGE UNIT
23
TARGET SLEW INFORMATION STORAGE UNIT
24
LATCH INFORMATION STORAGE UNIT
25
16
HOST COMPUTER
15
INTERFACE
18
ROM
RAM
19

FIG. 3A

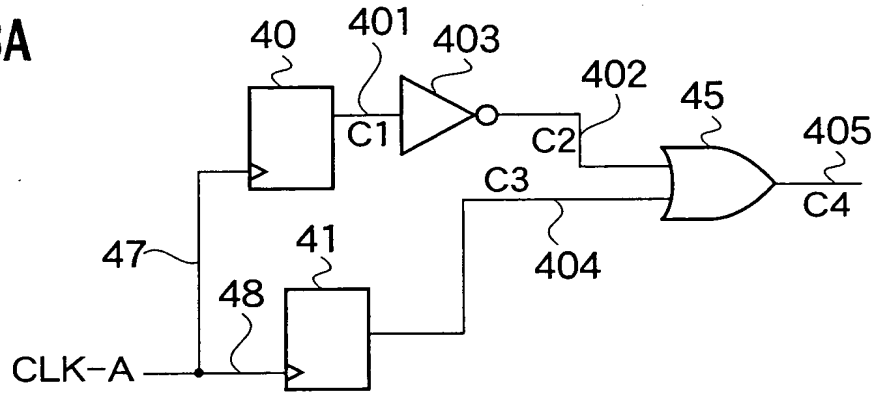


FIG. 3B

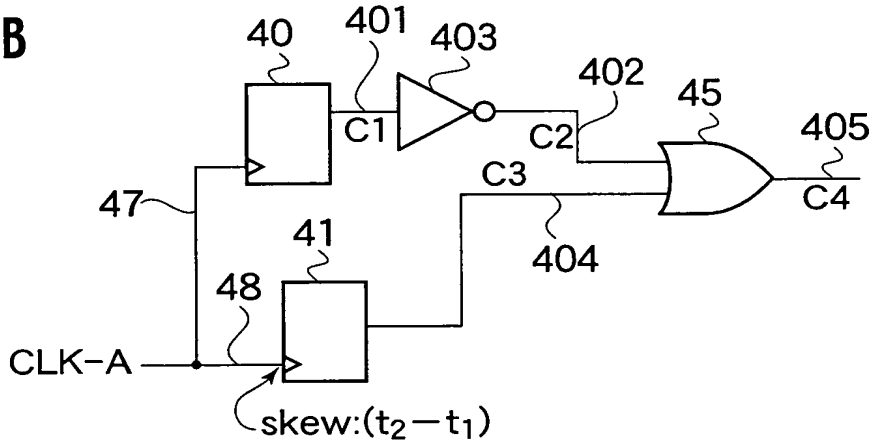


FIG. 3C

FIG. 3 D

FIG. 3E

FIG. 3F

FIG. 3G

FIG. 3H

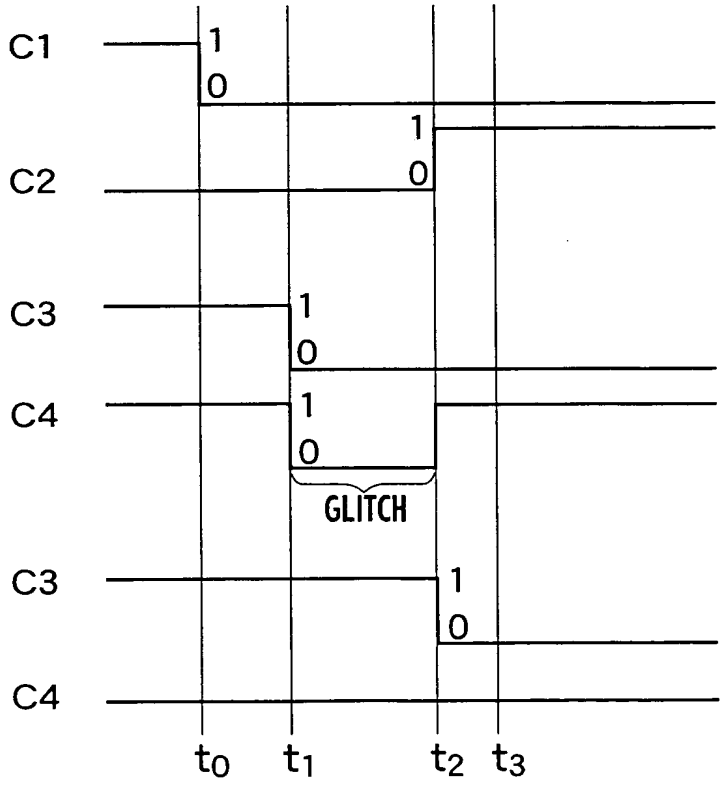


FIG.4A

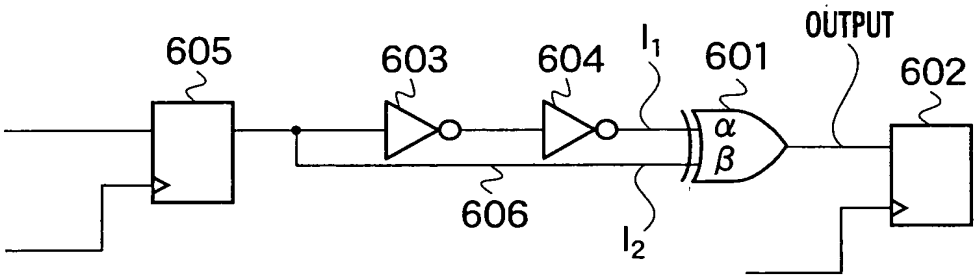


FIG. 4B

FIG. 4C

FIG. 4D

FIG. 4E

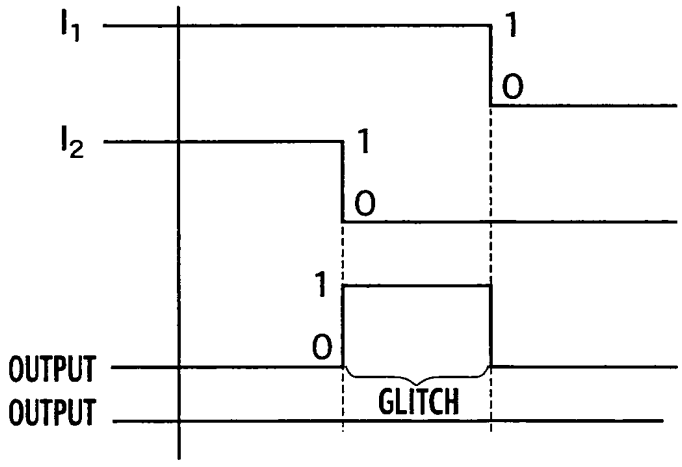


FIG. 5A

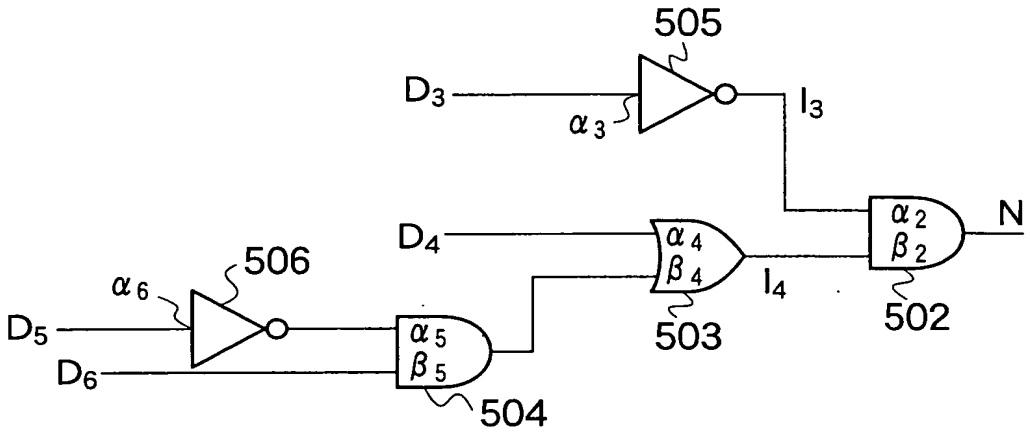

505
D3
α3
I3
D4
α4
β4
I4
α2
β2
N
502
503
506
α6
D5
D6
α5
β5
504

FIG. 5B

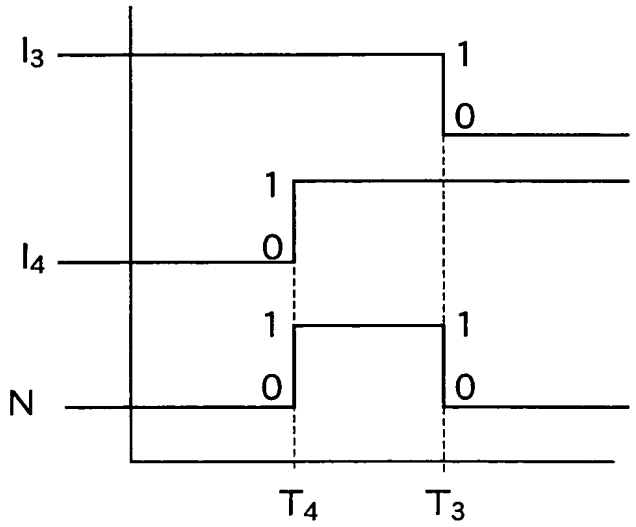

I3
1
0
I4
1
0
N
1
0
1
0
T4
T3

FIG. 6

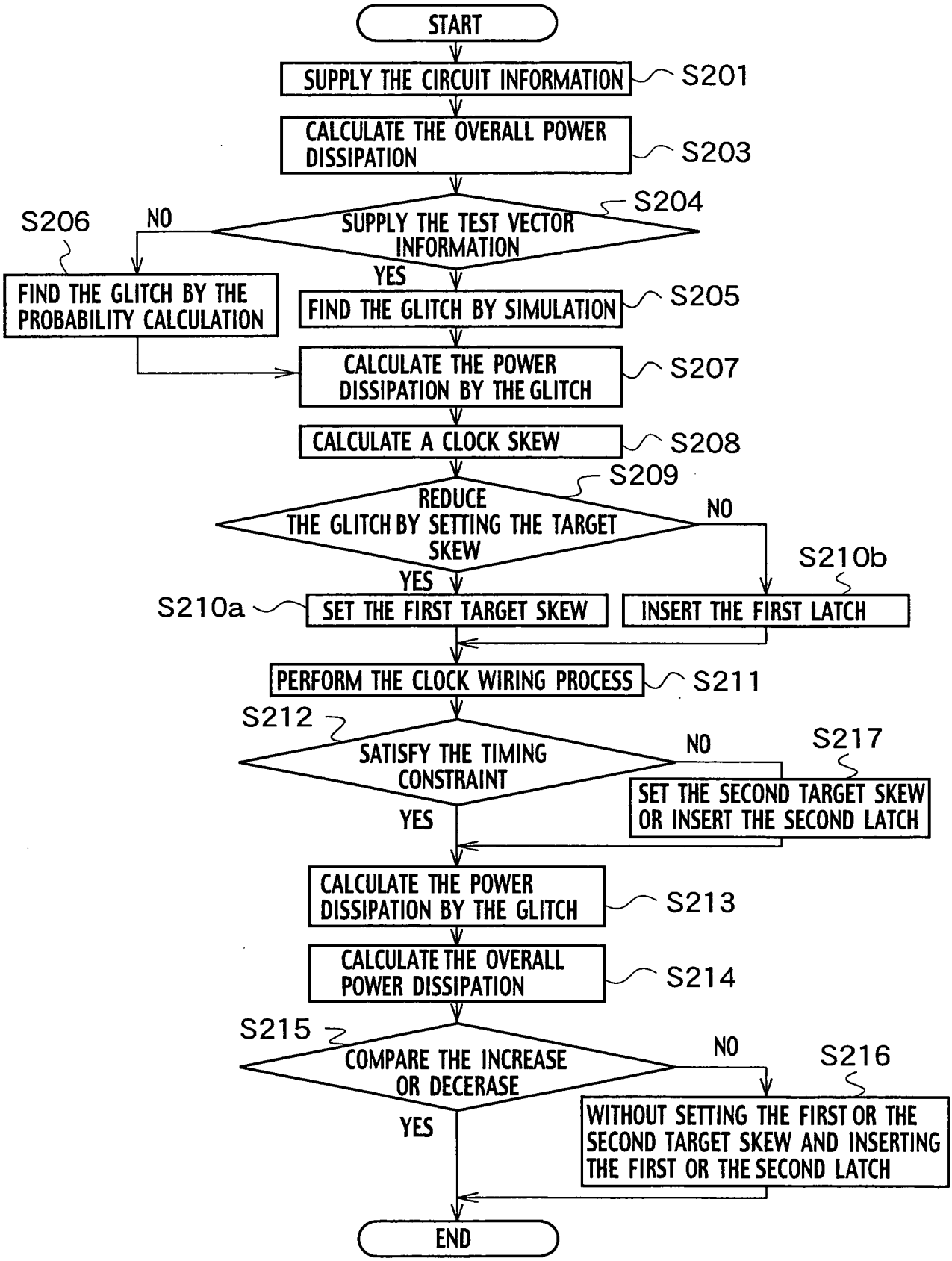

START
SUPPLY THE CIRCUIT INFORMATION
S201
CALCULATE THE OVERALL POWER DISSIPATION
S203
SUPPLY THE TEST VECTOR INFORMATION
S204
NO
S206
FIND THE GLITCH BY THE PROBABILITY CALCULATION
YES
FIND THE GLITCH BY SIMULATION
S205
CALCULATE THE POWER DISSIPATION BY THE GLITCH
S207
CALCULATE A CLOCK SKEW
S208
REDUCE THE GLITCH BY SETTING THE TARGET SKEW
S209
NO
S210b
YES
S210a
SET THE FIRST TARGET SKEW
INSERT THE FIRST LATCH
PERFORM THE CLOCK WIRING PROCESS
S211
S212
SATISFY THE TIMING CONSTRAINT
NO
S217
SET THE SECOND TARGET SKEW OR INSERT THE SECOND LATCH
YES
CALCULATE THE POWER DISSIPATION BY THE GLITCH
S213
CALCULATE THE OVERALL POWER DISSIPATION
S214
S215
COMPARE THE INCREASE OR DECERASE
NO
S216
YES
WITHOUT SETTING THE FIRST OR THE SECOND TARGET SKEW AND INSERTING THE FIRST OR THE SECOND LATCH
END

FIG. 7

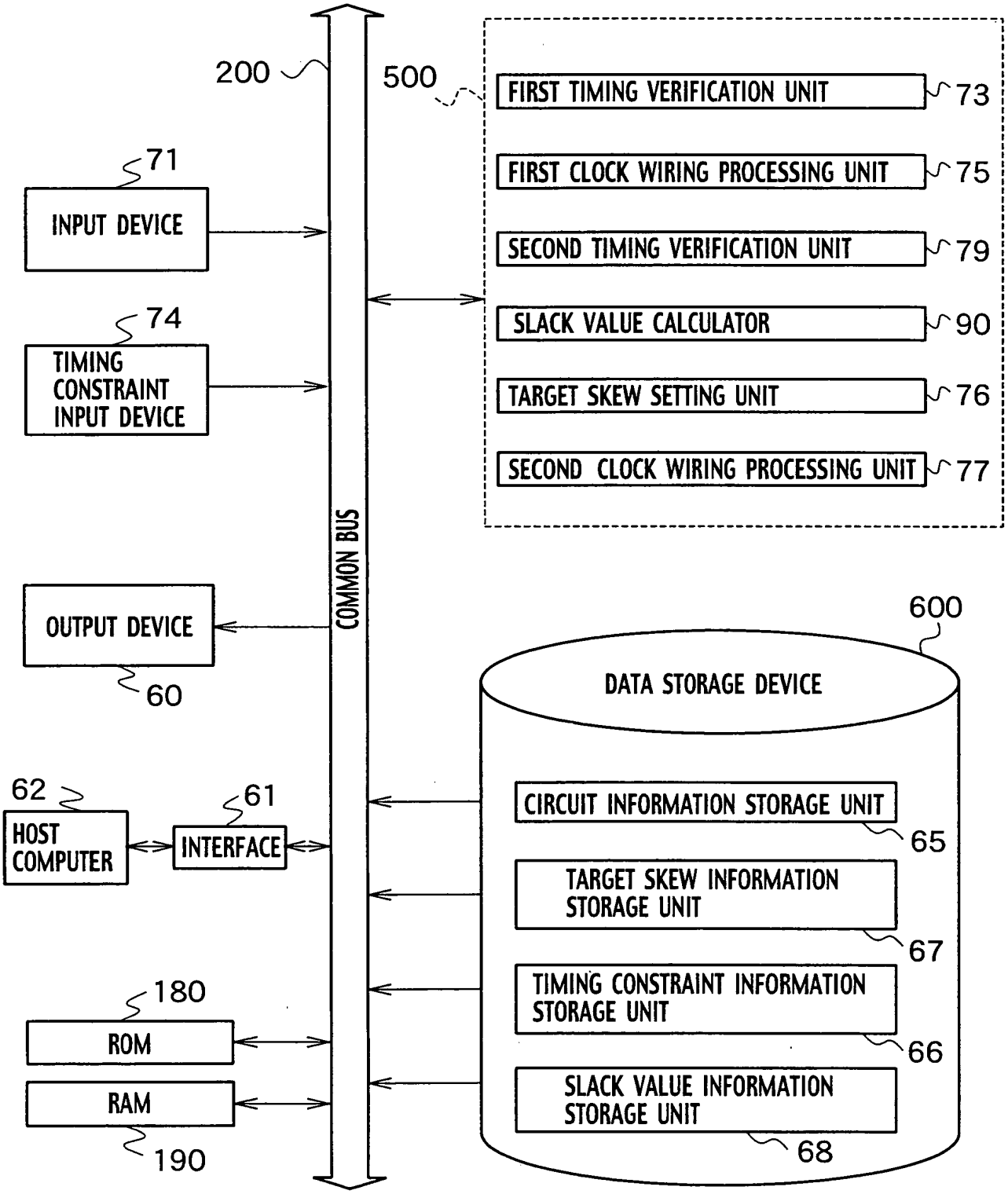

200
500
FIRST TIMING VERIFICATION UNIT
73
71
INPUT DEVICE
FIRST CLOCK WIRING PROCESSING UNIT
75
SECOND TIMING VERIFICATION UNIT
79
74
TIMING CONSTRAINT INPUT DEVICE
SLACK VALUE CALCULATOR
90
TARGET SKEW SETTING UNIT
76
SECOND CLOCK WIRING PROCESSING UNIT
77
COMMON BUS
600
OUTPUT DEVICE
60
DATA STORAGE DEVICE
62
61
HOST COMPUTER
INTERFACE
CIRCUIT INFORMATION STORAGE UNIT
65
TARGET SKEW INFORMATION STORAGE UNIT
67
180
TIMING CONSTRAINT INFORMATION STORAGE UNIT
66
ROM
SLACK VALUE INFORMATION STORAGE UNIT
RAM
68
190

FIG. 8

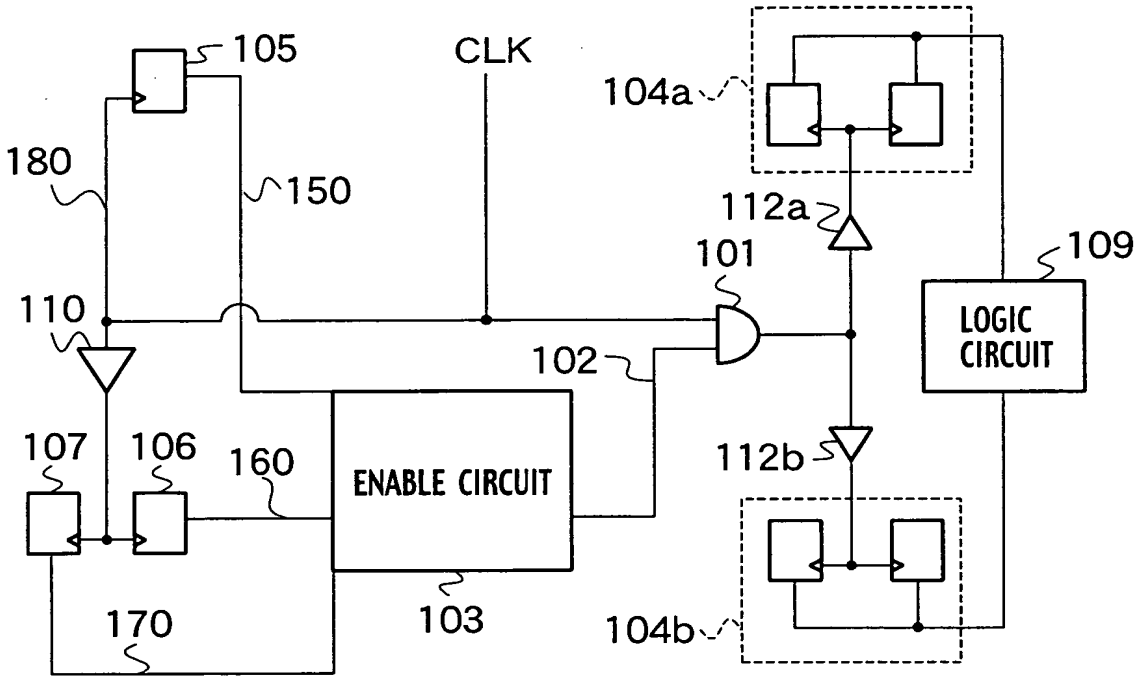
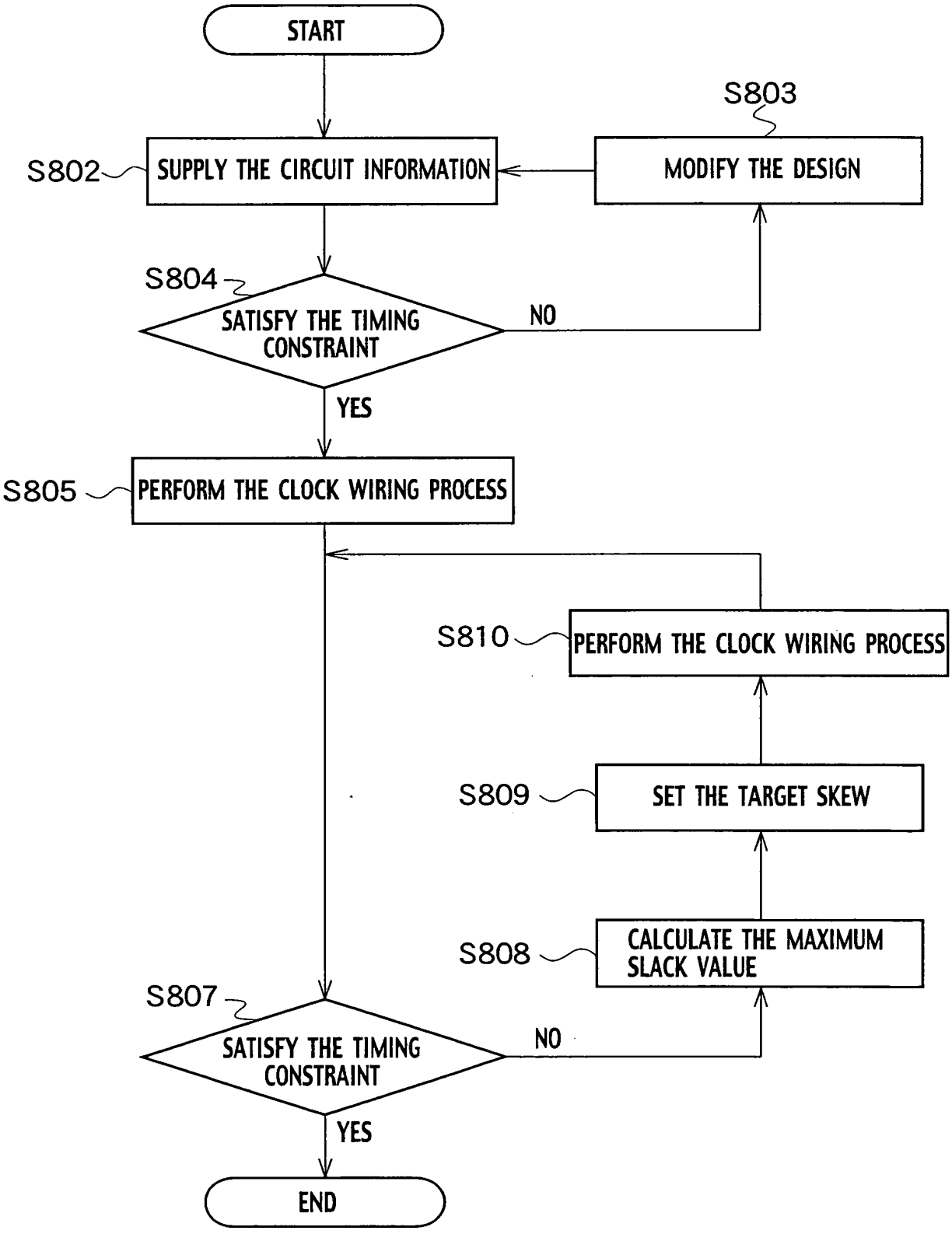

105
CLK
104a
180
150
112a
101
109
110
LOGIC CIRCUIT
102
107
106
160
ENABLE CIRCUIT
112b
170
103
104b

FIG. 9


START
S803
S802
SUPPLY THE CIRCUIT INFORMATION
MODIFY THE DESIGN
S804
SATISFY THE TIMING CONSTRAINT
NO
YES
S805
PERFORM THE CLOCK WIRING PROCESS
S810
PERFORM THE CLOCK WIRING PROCESS
S809
SET THE TARGET SKEW
S808
CALCULATE THE MAXIMUM SLACK VALUE
S807
SATISFY THE TIMING CONSTRAINT
NO
YES
END